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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,309	11/17/2003	Ketan Padalia	015114-069200US	6902

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EXAMINER	
LAM, NELSON C	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/716,309	PADALIA ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 11/17/2003. Application 10/716,309 has been examined. In the examination of 10/716,309, claims 1-26 are pending.

Specification

2. The disclosure is objected to because of the following informalities: On page 4, line 10, "step 104" should be "step 103" and on page 7, line 22, "adder circuit 401" should be "adder circuit 402".

Appropriate correction is required.

Claim Objections

Claims 1 and 9 are objected to because of the following informalities: As per claim 1 on page 15, line 6, the sentence containing "a logic block in response to" should be changed to "the logic block in response to". As per claim 9, on page 16, lines 1 and 4, the term "the logic blocks" has no antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the **first** paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 14-26 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. As to claim 14 in the specification, the applicant does not support or define the meaning of the term "code".

Claims 15-26 depend from rejected claim 14 and include all of the limitations of claim 14 thereby rendering these dependent claims indefinite.

5. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 9 and 12 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 9, the variable "k" is undefined (e.g., the variable k could be integers, real numbers, etc.).

Claim 9 recites the limitation "the logic blocks" on line 1 and "the logic block" on line 4. There is insufficient antecedent basis for this limitation in the claim.

As per claim 12, it is unclear how the existing placement information includes data that cannot exist until after the user design data is placed.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1-26 are rejected under 35 U.S.C. 103(a)** as being unpatentable over DiGiacomo et al U.S. Patent No. 4,630,219.

9. As per **claim 1**, DiGiacomo discloses a method for placing circuit elements into logic blocks, the method comprising:

assigning each of the circuit elements to a separate abstract block, wherein the circuit elements are part of a user design for a programmable integrated circuit (col. 2, line 44-50);

grouping each of the abstract blocks into a logic block (col. 2, line 50-54) ;

removing a first one of the abstract blocks from a logic block in response to placement information that indicates a design goal would be improved by rearranging at least a portion of the user design (Fig. 13; Fig. 46A; Fig. 46B; col. 9, line 43-59;); and

placing the first abstract block into a different logic block on the programmable integrated circuit (col. 29, line 27-43; col. 29, line 50-57).

As per **claim 2**, DiGiacomo discloses the method according to claim 1 wherein the design goal includes routability and signal timing in the user design (col. 8, line 3-10; col. 8, line 13-28).

As per **claim 3**, DiGiacomo discloses the method according to claim 1 wherein the circuit elements include lookup tables and registers (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit lookup tables and registers).

As per **claim 4**, DiGiacomo discloses the method according to claim 1 wherein the circuit elements include DSP blocks and RAM blocks (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit DSP blocks and RAM blocks).

As per **claim 5**, DiGiacomo discloses the method according to claim 1 further comprising:

determining whether placing each circuit element into the logic block violates any of a set of design rules relating to the logic block, wherein the logic blocks are grouped into clusters (Fig. 1, #12, #13; col. 6, line 25-42; Fig. 2, #22; col. 7, line 7-16); and

determining whether placing each of the circuit elements into a cluster violates any of a set of design rules relating to the cluster (Fig. 2, #22; Fig. 17; col. 11, line 51-53; col. 11, line 22-38, where the designs rules are the connectivity matrix).

As per **claim 6**, DiGiacomo discloses the method according to claim 5 wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of nets and connections of nets absorbed into the cluster if the abstract block is placed inside the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 7**, DiGiacomo discloses the method according to claim 5 wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of timing critical connections absorbed into the cluster if the abstract block is placed inside the cluster (col. 3, line 47-68; col. 4, line 1-7; col. 8, line 3-10; col. 28, line 12-16).

As per **claim 8**, DiGiacomo discloses the method according to claim 5 further comprising:

placing one of the abstract blocks into another logic block within the cluster if placing that abstract block into the logic block violates any of the design rule relating to

the logic block (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix), and

placing one of the abstract blocks into another cluster if placing that abstract block into the cluster violates any of the design rules relating to the cluster (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 9**, DiGiacomo discloses the method according to claim 1 wherein the logic blocks implement functions performed by two lookup tables with less than k unique input variables (col. 10, line 41-50); and the method further comprises:

determining whether placing each of the abstract blocks into the logic blocks causes any of the logic blocks to have more than k unique input variables (Fig. 6; col. 7, line 65-68; col. 8, line 1-3).

As per **claim 10**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes floorplanning information (Fig. 9; col. 9, line 27-31).

As per **claim 11**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes partition information (Fig. 17, #15; Fig. 21; Fig. 19B; col. 14, line 30-53).

As per **claim 12**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes data obtained by placing a portion of the user design on the programmable integrated circuit (Fig. 22, #82, #83; col. 15, line 19-30; col. 21, line 66-68; col. 22, line 1-22).

As per **claim 13**, DiGiacomo discloses the method according to claim 1 wherein:

grouping each of the abstract blocks into a logic block further comprises grouping first and second abstract blocks into a first logic block:

removing the first one of the abstract blocks from the logic block further comprises removing the first abstract block from the first logic block (col. 3, line 26-46; col. 4, line 8-17); and

placing the first abstract block into a different logic block further comprises placing the first abstract block into a second logic block and placing the second abstract block into the first logic block (col. 4, line 18-30).

As per **claim 14**, DiGiacomo discloses a computer program product stored on a computer readable medium for placing circuit elements in a user design for a programmable integrated circuit into logic blocks (Fig. 1, #14, #16; col. 1, line 6-13; col. 6, line 19-24), the computer program product comprising:

code for assigning each of the circuit elements to a separate abstract block (col. 2, line 44-50);

code for grouping each of the abstract blocks into a logic block (col. 2, line 50-54);

code for determining whether placement information indicates that a design goal would be improved by moving at least one of the abstract blocks into a different logic block (col. 29, line 27-43; col. 29, line 50-57); and

code for removing the at least one abstract block from a first logic block and placing the at least one abstract block into a second logic block in response to the

determination based on the placement information (Fig. 13; Fig. 46A; Fig 46B; col. 9, line 43-59).

As per **claim 15**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the design goal includes signal timing and routability in the user design (col. 8, line 3-10; col. 8, line 13-28).

As per **claim 16**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the logic blocks are grouped into clusters of logic blocks, and the code for grouping each of the abstract blocks into a logic block further comprises code for grouping each of the abstract blocks into a cluster of logic blocks based on an attraction of the abstract block to the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 17**, DiGiacomo discloses the computer program product as defined in claim 16 further comprising:

code for determining whether grouping the abstract blocks into the clusters violates any design rules of the clusters (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix); and

code for determining whether grouping the abstract blocks into the logic blocks violates any design rules of the logic blocks (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 18**, DiGiacomo discloses the computer program product as defined in claim 14 wherein some of the circuit elements are lookup tables, and some of the

circuit elements are registers (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit lookup tables and registers).

As per **claim 19**, DiGiacomo discloses the computer program product as defined in claim 16 wherein the attraction measures a number of nets and connections of nets absorbed into the cluster if the abstract block is placed inside the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 20**, DiGiacomo discloses the computer program product as defined in claim 16 wherein the attraction measures a number of timing critical connections absorbed into the cluster if the abstract block is placed inside the cluster (col. 3, line 47-68; col. 4, line 1-7; col. 8, line 3-10; col. 28, line 12-16).

As per **claim 21**, DiGiacomo discloses the computer program product as defined in claim 17 further comprising:

code for placing one of the abstract blocks into another logic block if placing that abstract block to the logic block violates any of the design rules relating to the logic block (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 22**, DiGiacomo discloses the computer program product as defined in claim 17 further comprising:

code for placing one of the abstract blocks to another cluster if placing that abstract block to the first cluster violates any of the design rules relating to the first cluster (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 23**, DiGiacomo discloses the computer program product as defined in claim 14 further comprising:

code for determining whether placing the abstract blocks to the logic blocks causes any of the logic blocks have more than k unique input variables (col. 10, line 41-50),

wherein the logic blocks are configurable to implement functions performed by two lookup tables with less than k unique input variables (Fig. 6; col. 7, line 65-68; col. 8, line 1-3).

As per **claim 24**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes floorplanning information (col. 3, line 44-50).

As per **claim 25**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes partition information (col. 21, line 9-26).

As per **claim 26**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes data obtained by placing logic blocks that implement portions of the user design on the programmable integrated circuit (Fig. 22, #82, #83; col. 15, line 19-30; col. 21, line 66-68; col. 22, line 1-22).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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